2829

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Matsumoto Toshiyuki et al.		
Serial No.:	09/703,845	Art Unit:	2829
Filed:	November 2, 2000	Examiner:	Nguyen, Tung X.
For:	CAPACITANCE MEASUREMENT METHOD OF MICRO STRUCTURES OF INTEGRATED CIRCUITS		

AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the official Office Action dated December 30, 2003, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please see the changes to the specification attached hereto.

IN THE CLAIMS

Please see the Claim Summary Document attached hereto.

REMARKS

In response to the official Office Action dated December 30, 2003, Applicant has amended the claims and specification to clarify the areas noted by the examiner. Applicant has changed all references to "potential" such that there is no confusion between "potential" and "voltage." Non-elected Claims 23-25 have been canceled but are not being abandoned. They will be the subject of a divisional application.

With respect to the rejection of Claim 20 under 35 U.S.C. § 112, Claim 20 has been amended to clarify that a common potential is applied to the gate, channel area and the other of the source and drain if the bias potential is applied to one of the source or drain. Alternatively, the common potential is applied to one of the source and drain, the other of the source or drain and the channel region if the biasing potential is applied to the gate. The essence is that there is to be a measurement between the gate and one of the source and drain.